

What is claimed is:

- 1 1. An apparatus, comprising:
2 a semiconductor device formed on a conductivity region; and
3 a low resistive path barrier formed surrounding the conductivity region to isolate the
4 conductivity region from a substrate that supports the conductivity region and the low
5 resistive path barrier.
- 1 2. The apparatus of claim 1, further comprises of a deep trench isolation formed
2 surrounding the low resistive path barrier on the opposite side of the conductivity region.
- 1 3. The apparatus of claim 2, wherein the deep trench isolation extends into the
2 substrate.
- 1 4. The apparatus of claim 1, wherein the conductivity region is at least one of n-type
2 and p-type conductivity regions.
- 1 5. The apparatus of claim 1, wherein the semiconductor device is a selected one of
2 CMOS, BiCMOS, NMOS and PMOS.
- 1 6. The apparatus of claim 1, wherein the low resistive path barrier is coupled to a
2 power supply.
- 1 7. The apparatus of claim 1, wherein the substrate is selected from one of p-type
2 and n-type substrate.
- 1 8. The apparatus of claim 1, wherein the low resistive path barrier comprises of a
2 plug coupled to a buried layer.

- 1 9. The apparatus of claim 8, wherein the plug is coupled to a power supply.
- 1 10. The apparatus of claim 1, wherein the low resistive path barrier comprises a
2 selected one of N+ and P+ doped material.
- 1 11. The apparatus of claim 1, wherein the deep trench isolation comprises of a
2 selected one of a dielectric and an insulation material.
- 1 12. The apparatus of claim 1, wherein the substrate is biased to 0 volts.
- 1 13. The apparatus of claim 1, wherein the low resistive path barrier comprises of a
2 first capacitive decoupling junction located at an interface between the low resistive path
3 barrier and the conductivity region, and a second capacitive decoupling junction located
4 at an interface between the low resistive path barrier and the substrate.
- 1 14. The apparatus of claim 7, wherein the plug having a resistivity of about 0.01
2 ohm-cm and the buried layer having a resistivity of about 0.005 ohm-cm.
- 1 15. The apparatus of claim 2, wherein the deep trench isolation having a depth of
2 about 5 μm .
- 1 16. A method comprising:
2 forming a semiconductor device on a conductivity region; and
3 forming a low resistive path barrier that surrounds the conductivity region to isolated the
4 conductivity region from a substrate that supports the conductivity region and the low
5 resistive path barrier,

- 1 17. The method of claim 16, further comprises forming a deep trench isolation
2 surrounding the low resistive path barrier on the opposite side of the conductivity region.
- 1 18. The method of claim 16, further comprises coupling the low resistive path barrier
2 to a power supply.
- 1 19. The method of claim 16, wherein the semiconductor device is a selected one of
2 CMOS, BiCMOS, NMOS and PMOS.
- 1 20. The method of claim 16, wherein the conductivity region is at least one of n-type
2 and p-type conductivity regions.
- 1 21. The method of claim 16, wherein the formed low resistive path barrier comprises
2 a plug coupled to a buried layer.
- 1 22. The method of claim 21, further comprises coupling the plug to a power supply.
- 1 23. The method of claim 17, wherein forming of deep trench isolation further
2 comprises filling the deep trench isolation with a selected one of a dielectric or a
3 insulation material.
- 1 24. The method of claim 16, wherein the formed low resistive path barrier comprises
2 a selected one of N+ and P+ doped material.
- 1 25. A system, comprising:
2 an integrated circuit having a semiconductor device formed on a conductivity
3 region, including

4 a low resistive path barrier formed surrounding the conductivity region to isolated the
5 conductivity region from a substrate that supports the conductivity region and the low
6 resistive path barrier;
7 a bus coupled to the integrated circuit; and
8 a networking interface coupled to the bus.

1 26. The system of claim 25, further comprises a deep trench isolation formed
2 surrounding the low resistive path barrier on the opposite side of the conductivity region;

1 27. The system according to claim 25, wherein the low resistive path barrier is
2 coupled to a power supply.

1 28. The system according to claim 25, wherein the semiconductor device is selected
2 from one of CMOS, BiCMOS, NMOS and PMOS.

1 29. The system according to claim 25, wherein the low resistive path barrier
2 comprises a selected one of N+ and P+ doped material.

1 30. The system according to claim 25, wherein the low resistive path barrier
2 comprises of a plug and a buried layer.